

WHAT IS CLAIMED IS:

1 1. A method of forming a rough topology on a
2 substrate using a planarized process comprising the steps of:
3 forming a contact opening having a lateral dimension
4 exceeding a minimum contact size;
5 filling the contact opening with a first plug layer;
6 etching back the first plug layer to create a first
7 cored region in the first plug layer, whereby the first cored
8 region has a first depression; and
9 stacking a first subsequent process layer on the
10 first cored region, whereby the first subsequent process layer
11 has a second depression formed on top of the first depression.

1 2. The method of claim 1 further comprising the
2 steps of:
3 forming a first via opening on the contact opening;
4 filling the first via opening with a second plug
5 layer;
6 etching back the second plug layer to create a
7 second cored region in the second plug layer, wherein the
8 second cored region has a third depression formed on top of
9 the second depression; and
10 stacking a second subsequent process layer on the
11 second cored region, wherein the second subsequent process
12 layer has a fourth depression formed on top of the third
13 depression.

1 3. The method of claim 2 further comprising the
2 steps of:
3 forming a second via opening on the first via
4 opening and the contact opening;
5 filling the second via opening with a third plug
6 layer; and
7 etching back the third plug layer to create a third
8 cored region in the third plug layer, wherein the third cored
9 region has a fifth depression formed on top of the fourth
10 depression.

1 4. The method of claim 1 wherein the contact
2 opening is formed on a polysilicon layer.

1 5. The method of claim 1 wherein the first
2 depression has a different optical reflectivity compared to a
3 relatively planar region of the substrate.

1 6. The method of claim 1 wherein the second
2 depression forms a rough, nonplanar topology to scatter
3 incident radiation, resulting in a dissimilar optical
4 reflectiveness from a smooth topology of the substrate.

1 7. The method of claim 1 further comprising the
2 steps of:

3 forming an insulating layer on the substrate and
4 covering the first cored region; and

5 removing portions of the insulating layer covering
6 the first cored region, thereby enhancing an optical contrast
7 between the second depression and a planar region of the
8 substrate.

1 8. The method of claim 1 wherein the first
2 subsequent process layer is a first metal layer.

1 9. The method of claim 2 wherein the second
2 subsequent process layer is a second metal layer.

1 10. The method of claim 1 further wherein the
2 lateral dimension is at least about 1.5 times larger than the
3 minimum contact size.

1 11. The method of claim 1 wherein a shape of the
2 contact opening is rectangular.

1 12. An alignment structure formed in a planarized
2 semiconductor process comprising:

3 a substrate;
4 a contact opening formed on the substrate;
5 a first plug layer filling the contact opening, the
6 first plug layer having a first depressed region in the
7 contact opening, whereby a topological roughness formed by the
8 first depressed region scatters incident radiation.

1 13. The alignment structure of claim 12 wherein the
2 topological roughness contrasts reflectively to a
3 topologically smooth region.

1 14. The alignment structure of claim 12 wherein the
2 first depressed region is in about a middle of the contact
3 opening.

1 15. The alignment structure of claim 12 further
2 comprising:

3 a first via opening stacked on top of the contact
4 opening, whereby the first via opening enhances the
5 topological roughness formed by the first depressed region.

1 16. The alignment structure of claim 15 further
2 comprising:

3 a second via opening stacked on top of the first via
4 opening and second via opening, whereby the second via opening
5 further enhances the topological roughness.

1 17. The alignment structure of claim 12 wherein the
2 contact opening is larger than a minimum size specified by a
3 design rule.

1 18. An alignment structure for semiconductor
2 fabrication comprising:
3 a smooth region formed on a substrate;
4 a rough region formed on the substrate comprising:
5 a first conductive layer;
6 a second conductive layer formed above the
7 first conductive layer,
8 an first insulating layer, between the
9 first and second conductive layers, wherein the
10 first insulating layer has a first opening for
11 electrically coupling the first and second
12 conductive layers;
13 a plug layer filling the first opening,
14 wherein the first plug layer has a cored
15 region, whereby a topological roughness formed
16 by the cored region scatters incident
17 radiation.

1 19. The alignment structure of claim 18 wherein the
2 rough region further comprises:

3 a third conductive layer formed above the second
4 conductive layer;

5 a second insulating layer, between the second and
6 third conductive layers, wherein the second conductive layer
7 has a second opening, stacked above the first opening, for
8 electrically coupling the third and second conductive layers,
9 whereby the second opening aggravates the topological
10 roughness formed by the cored region.

1 20. The alignment structure of claim 18 wherein the
2 cored region creates a void above the cored region and second
3 conductive layer.

1 21. The alignment structure of claim 19 wherein the
2 opening has a lateral dimension at least about 1.5 times
3 larger than a minimum size.

1 22. The alignment structure of claim 19 wherein a
2 passivation layer, covering the substrate, is removed from the
3 rough region to enhance a reflectivity contrast between the
4 rough region and smooth region.

1 23. The alignment structure of claim 19 wherein the
2 smooth region is adjacent to the rough region.

1 24. The alignment structure of claim 19 wherein the
2 smooth region is formed using a metal layer.